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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ward D. Parkinson, et al.	§	Group Art Unit:	2827
Serial No.:	10/634,153	§	Examiner:	Viet Nguyen
Filed:	August 4, 2003	§		
For:	Analog Phase Change Memory	§	Atty. Dkt. No.:	ITO.0553US (P16341)

Mail Stop **Appeal Brief**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF AMENDED APPEAL BRIEF

Dear Sir:

In response to the Notification of Non-Compliant Appeal Brief, attached hereto is an Amended Appeal Brief.

Statute and reference information has been added to the Grounds of Rejection section and the headings of the Arguments section of this Appeal Brief. The Amended Appeal Brief is therefore believed to be in compliance.

No fee is believed to be due with this response. However, the Commissioner is authorized to charge any fee due to Deposit Account No. 20-1504 (ITO.0553US).

Respectfully submitted,

Date: October 12, 2006

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Date of Deposit: October 12, 2006
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Nancy Meshkoff

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Ward D. Parkinson	Art Unit:	2827
Serial No.:	10/634,153	Examiner:	Viet Q. Nguyen
Filed:	August 4, 2003	Atty Docket:	ITO.0553US (P16341)
For:	Analog Phase Change Memory	Assignee:	Intel Corporation

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AMENDED APPEAL BRIEF

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Nancy Meshkoff

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REAL PARTY IN INTEREST

The real party in interest is the assignee Ovonyx, Inc.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-25 (Rejected).

Claims 1-25 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. A method comprising:

forming an analog memory (50, Figure 2, specification at page 4, lines 12-23) using a phase change material (42, Figure 2, specification at page 4, lines 12-23).

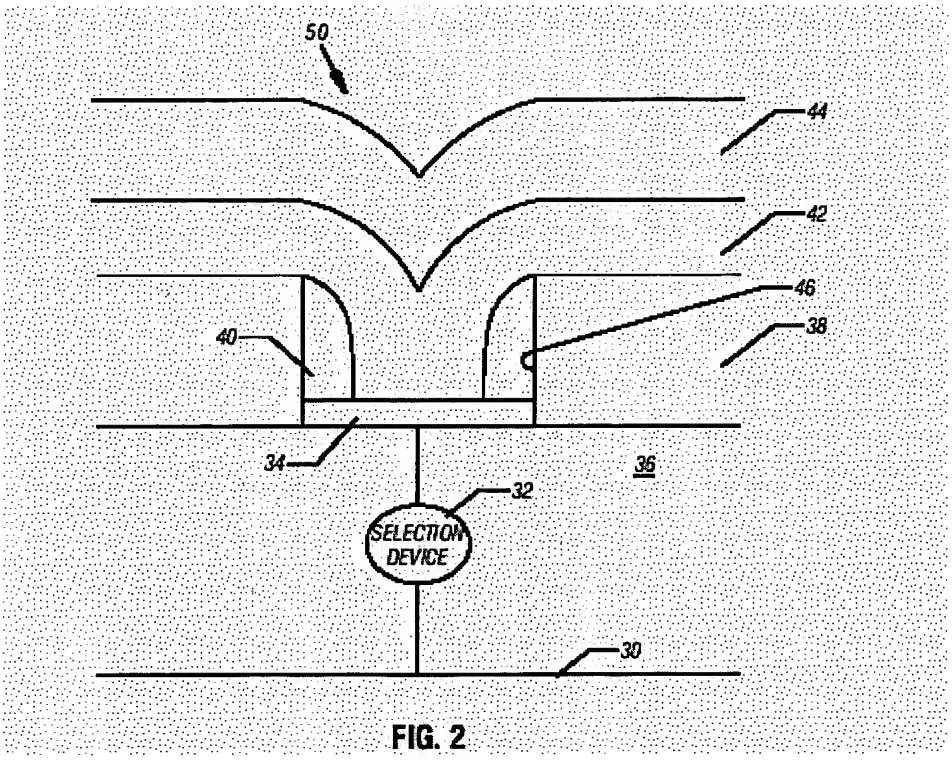

FIG. 2

11. A memory comprising:

a phase change material (42, Figure 2, specification at page 4, lines 12-23); and

a circuit (22, Figure 1, specification at page 3, lines 15-20) to write analog data using said phase change material.

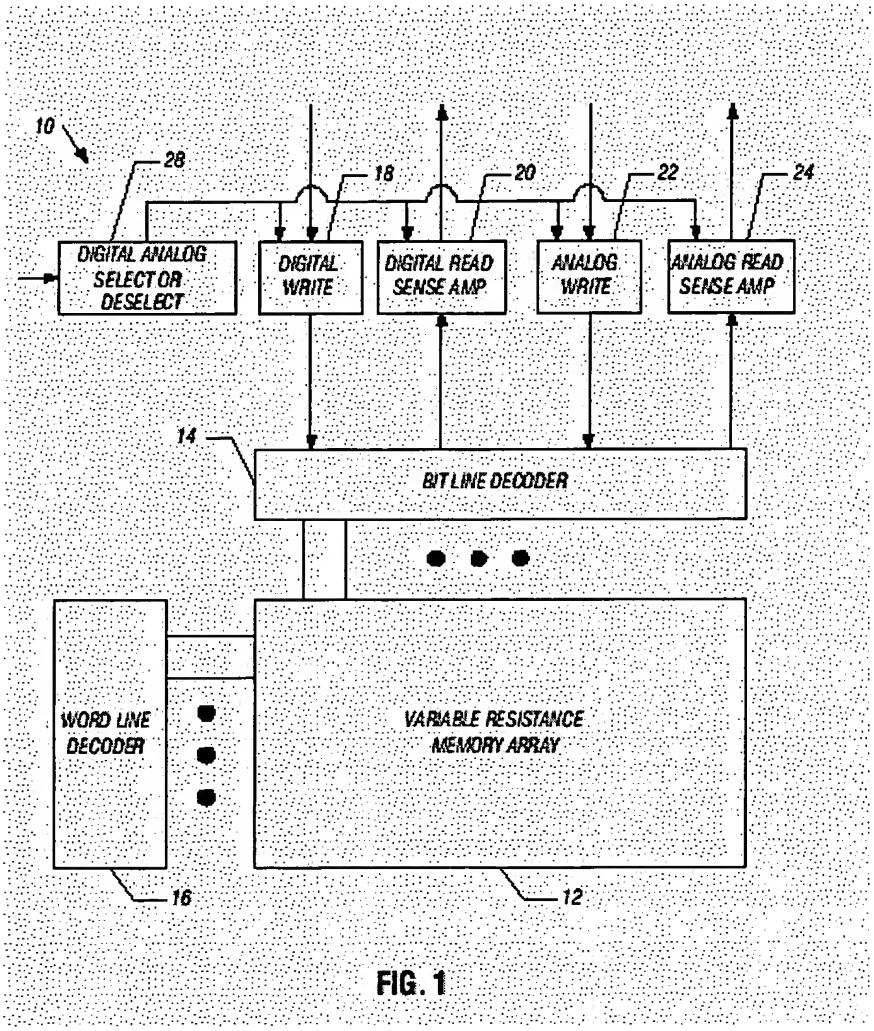

FIG. 1

21. A system comprising:

a processor (510, Figure 3, specification at page 10, lines 22-24);

a wireless interface (540, Figure 3, specification at page 10, lines 16-21) coupled to said processor; and

a semiconductor memory (530, Figure 3, specification at page 4, lines 12-23) coupled to said processor, said memory including a phase change material (412, Figure 2, specification at page 4, lines 12-23) and a circuit (22, Figure 1, specification at page 3, lines 15-20) to write analog data for storage using said phase change material.

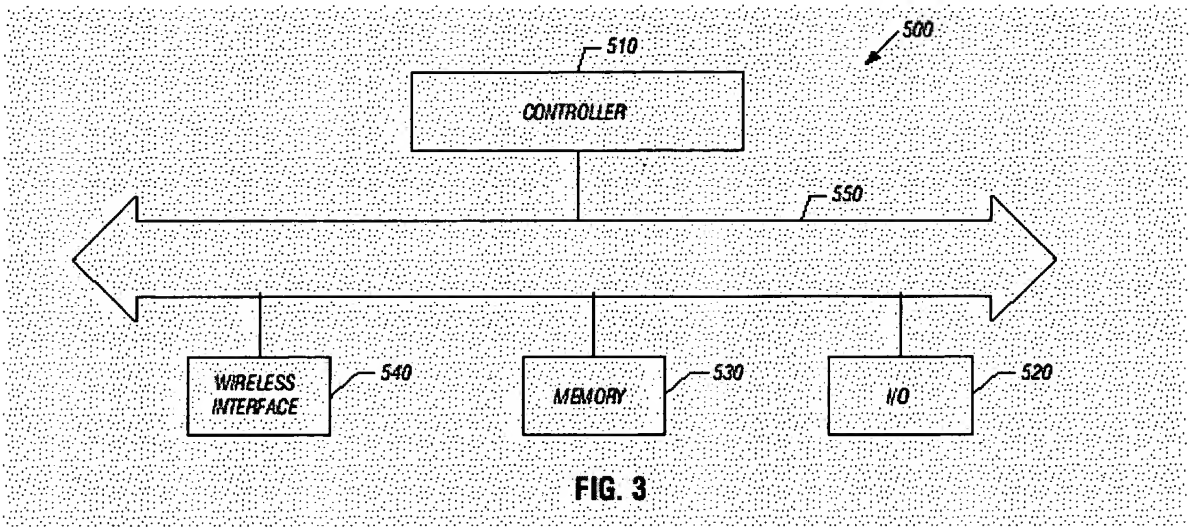

FIG. 3

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. **Are claims 2, 11, 12, 14-16, and 22-25 indefinite under 35 U.S.C. § 112, second paragraph for failing to particularly point out and distinctly claim the subject matter of the invention?**

B. **Are claims 1-25 unpatentable under U.S.C. § 103(a) over Ovshinsky (RE37,259)?**

C. **Are claims 1-25 unpatentable under U.S.C. § 103(a) over Klersy (5,933,365)?**

D. **Are claims 1-25 unpatentable under U.S.C. § 103(a) over Czubatyj (5,825,046)?**

E. **Are claims 1-25 unpatentable under U.S.C. § 103(a) over Van Brocklin (6,879,525)?**

F. **Are claims 1-25 unpatentable under U.S.C. § 103(a) over Czubatyj (4,782,340)?**

ARGUMENT

A. Are claims 2, 11, 12, 14-16, and 22-25 indefinite under 35 U.S.C. § 112, second paragraph for failing to particularly point out and distinctly claim the subject matter of the invention?

The belated assertion of a § 112 rejection should be reversed. The suggestion that the claim language is both vague and indefinite and impossible is internally inconsistent. The objection is not based on possibility or enablement but only for indefiniteness.

The claims are clear to any reasonable reading. They call for selectively enabling either digital or analog data to be stored. There is nothing vague about that language.

The specification is clear that analog and digital information can be selectively stored. The present brief shows such a structure in Figure 1 incorporated herein on page 8. There is a circuit which selectively enables digital or analog storage. It has a digital write circuit 18, a digital read sense amp 20, an analog write circuit 22, and an analog read sense amp 24, each of which can be selected by the digital analog select or deselect circuit 28. This is explained in the specification at page 3, lines 4-20.

There is nothing indefinite or impossible about it. The fact that the examiner thinks that it is impossible certainly militates against his own ensuing assertion of obviousness.

The assertion that claim 1, a method claim, only calls for forming an analog memory is noted, as pointed out in the Office action. But claim 1 and claim 2 are different claims. Claim 2 calls for selectively enabling either analog or digital data to be stored in that analog memory. The assertion that somehow this is hard to do without any major design changes or data format the specification.

Presumably since the examiner believes that the invention is obvious, he must believe that these capabilities are also enabled by the cited references. To the contrary, he apparently believes these same deficiencies exist in the cited references. Therefore this is additional grounds to reverse the plainly mistaken obviousness rejections, each taken over a single reference by itself, despite the fact that, according to the examiner, each reference fails to teach what is necessary to meet the claim limitations.

B. Are claims 1-25 unpatentable under U.S.C. § 103(a) over Ovshinsky (RE37,259)?

All of the claims are rejected under Section 103 over any one of Ovshinsky, Klersy, Czubatyj, Van Brocklin, or Czubatyj '340 or '046.

However, every one of these references relates to a digital system and not one of them relates to an analog system.

More particularly, each of them store states, not analog signals. States, regardless of the number of states, is commensurate with digital storage. There is no storage of states in analog storage.

With respect to Ovshinsky, it is pointed out that in the background prior art there is a discussion of an ovonic EEPROM that is capable of both analog and digital forms of information storage. However, the material pointed out by the Examiner indicates that what is referred to here is not storage of the analog signal itself, but storage of a representation, in digital form, of the analog signal. In other words, the analog signal is converted into gray scales or other digital representations and stored.

This is explicitly explained in column 1, lines 57-60, where there is a discussion of gray scale values. Gray scale is the digitization of the analog information. See the attachment to the previous response. This is further substantiated by the material at column 20, lines 56 *et. seq.,* talking about the dynamic range of resistance allows for broad "gray scale and multilevel analog memory storage." Thus, levels in gray scale teach digital storage of digitized analog information. Similarly, in column 20, line 61, it is explained that it is binary information that is stored in the cell. Further, multilevel storage, which preceded analog memory storage in line 57, is explained to be binary information in pseudo-analog form. Instead, analog levels are used and provided with the capability of storing n bits of binary information. There can be no doubt that analog information is converted to digital form (digitized) and this is what is being stored. While this is called analog storage, apparently because an analog signal is digitized and stored, it does not amount to storing an analog value as an analog value in the storage. While the reference's terminology is awkward and perhaps incorrect, the intent is clear.

C. Are claims 1-25 unpatentable under U.S.C. § 103(a) over Klersy (5,933,365)?

The Klersy patent appears to have the same information as the Ovshinsky patent and the same comments apply.

D. Are claims 1-25 unpatentable under U.S.C. § 103(a) over Czubatyj (5,825,046)?

The Czubatyj '046 patent appears to have the same information and the same comments apply.

E. Are claims 1-25 unpatentable under U.S.C. § 103(a) over Van Brocklin (6,879,525)?

The Van Brocklin patent also stores states. This is explicitly conceded in the second through the fourth line of page 6 of the office action and is clearly set forth in the Van Brocklin reference. If an analog signal is being stored there would be no states, be they multiple states or otherwise. Thus, in analog storage, level states are not stored, an analog signal is stored. The discussion of levels and states makes it absolutely clear that Van Brocklin is storing digitized representations of analog information.

For example, in column 5, lines 26-37, it is explained that for a given program state, there is a sensed current. There would not be states if analog storage was involved. Further, there is a discussion of four possible states and the note that any number of states could be implemented. In analog storage there would be no states. Clearly, the discussion is of digital storage. Similarly, with respect to the sense circuitry at column 5, lines 55-61, there is discussion of the detection of a particular value of an electrical parameter, plainly, a discussion of a digital storage device. Also, at column 5, lines 62-63, there is discussion of a memory cell that has one state-change device that can be programmed to multiple states.

Similarly, in connection with Figure 8, and column 9, lines 38 *et. seq.*, there is a discussion of states and programming to discrete states. Therefore, there can be no dispute that the information described in this reference involves digital storage. See, for example, claim 1 calling for a state change device, claim 11 calling for a state change device having at least three states, claim 21 calling for a state change device, and claim 31 calling for a state change device.

F. Are claims 1-25 unpatentable under U.S.C. § 103(a) over Czubatyj (4,782,340)?

The Czubatyj '340 patent suffers from the same deficiencies described above. The fact that at column 2, lines 25-35, there is discussion of electrically detectable forms does not militate against determining states. The only alternatives described in column 2, lines 30-35, is what is called a binary value, a logical one or a logical zero, or an analog value such as a gray scale value or other electrically detectable form. As pointed out before, and as explained in the attachment to the previous response, a gray scale value is a digitized analog form. Clearly, the reference teaches what might be loosely and incorrectly called storing analog information, but

doing so by digitizing that information. As such, the reference fails to meet the claim limitations.

Specifically, claim 1 calls for forming an analog memory using a phase change material. Claim 2 calls for selectively enabling digital or analog storage. None of the references enable selective digital or analog data to be stored, not only because they never store analog data in analog form, but because they do not allow such selectivity.

The Applicants' usage of analog non-volatile memory is consistent with that set forth in U.S. Patent 5,745,409 at column 1, lines 26-39 cited by Applicants. (See Evidence Appendix). This demonstrates that those skilled in the art understand that analog non-volatile memories are distinct from digital non-volatile memories and that they store analog, not digital, representations of analog information.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: October 12, 2006

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CLAIMS APPENDIX

The claims on appeal are:

1. A method comprising:
forming an analog memory using a phase change material.

2. The method of claim 1 including selectively enabling either digital or analog data to be stored in said memory.

3. The method of claim 1 including forming a phase change material having a programmably variable resistance for a plurality of cells.

4. The method of claim 3 including enabling said cells to be addressably located along rows and columns.

5. The method of claim 1 including forming a phase change material in a pore.

6. The method of claim 5 including forming a selection device to enable the control of current through said phase change material.

7. The method of claim 1 including enabling said memory to store in a single cell one of at least three different resistance values.

8. The method of claim 7 including enabling the resistance of the cell to be set by varying the magnitude of a programming current to the cell.

9. The method of claim 8 including enabling the resistance of the cell to read and readjust using a different programming current.

10. The method of claim 9 including enabling a resistance to be set in said cell proportional to a voltage or current characteristic to be stored.

11. A memory comprising:

a phase change material; and

a circuit to write analog data using said phase change material.

12. The memory of claim 11 including a circuit to selectively enable either digital or analog data to be stored in said memory.

13. The memory of claim 11 wherein said phase change material has a programmably variable resistance.

14. The memory of claim 13, said memory to store digital and analog data.

15. The memory of claim 14 wherein said memory to selectively store digital or analog data.

16. The memory of claim 15 including a circuit to enable a user to select analog or digital data storage.

17. The memory of claim 16 including an analog read sense amplifier, a digital read sense amplifier, an analog write circuit, and a digital write circuit.

18. The memory of claim 11 including a substrate, an insulator formed over said substrate, a pore defined in said insulator, and a phase change material in said pore.

19. The memory of claim 11 including a plurality of cells including a phase change material, said memory including a plurality of conductive lines to selectively enable access to said cells.

20. The memory of claim 19 wherein said phase change material includes a chalcogenide.

21. A system comprising:

a processor;

a wireless interface coupled to said processor; and

a semiconductor memory coupled to said processor, said memory including a phase change material and a circuit to write analog data for storage using said phase change material.

22. The memory of claim 21 including a circuit to selectively enable either digital or analog data to be stored in said memory.

23. The system of claim 21, said memory to store digital and analog data.

24. The system of claim 23 wherein said memory to selectively store digital or analog data.

25. The system of claim 24 including a circuit to enable a user to select analog or digital data storage.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.